REMARKS

This responds to the Office Action dated on August 9, 2007. No claims are amended, canceled or added. Thus, claims 1-53 and 66-69 remain pending in this application.

Allowable Subject Matter

Applicant thanks the Examiner for the finding of allowable subject matter.

Claims 22-38, 47-52 and 66-69 were allowed.

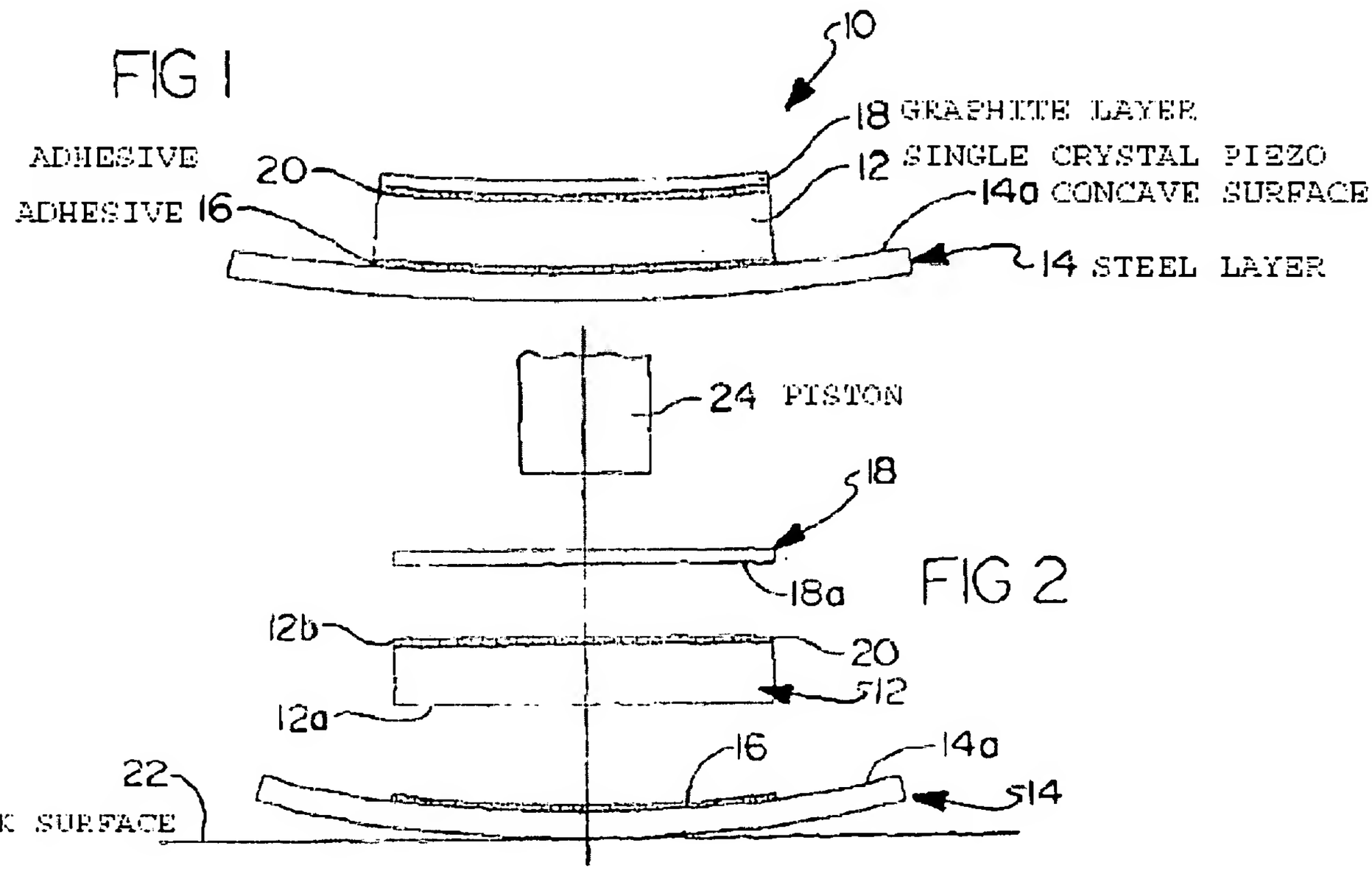
Claims 4, 8, 9, 15 and 42 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant respectfully asserts that the base claims for claims 4, 8, 9, 15 and 42 are in condition for allowance for the reasons that follow. As such, Applicant respectfully asserts that claims 4, 8, 9, 15 and 42 are also in condition for allowance.

§*103 Rejection of the Claims*

Claims 1-3, 6, 7, 12, 14 and 16-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Clingman et al. (U.S. Patent No. 6,994,762) in view of Belford (U.S. Patent No. 6,455,397). Applicant respectfully traverses for at least the following reasons.

The Office asserts that Clingman et al. shows "straightening the predetermined contour to induce a predetermined strain" in the single crystal piezo 12. Applicant respectfully disagrees.

The steel layer 14 is formed with a predetermined curvature[1], and the single crystal piezo material 12 is bonded to the steel layer 14 while the steel layer is held in a flattened condition[2]. Once bonding is complete, the force is removed and the steel layer is allowed to flex back into its predetermined curvature, causing a compressive prestrain to be applied to the SCP material as the steel layer assumes its original, predetermined curvature[3].



---

[1] *Clingman et al.*, at col. 1 line 67 to col. 2 line 2. *See also* col. 3 lines 16-18.
[2] *Clingman et al.*, at col. 2 lines 2-4. *See also* col. 3 lines 44-50.
[3] *Clingman et al.*, at col. 2 lines 4-8. *See also* col. 3 lines 19-21, 52-55.

Thus, Applicant asserts that the strain is not induced by straightening the predetermined contour, but rather the strain is caused when the steel layer flexes back to its original, preformed curvature. Therefore, Clingman et al. does not show "bonding the semiconductor membrane to the substrate wafer and straightening the predetermined contour to induce a predetermined strain in the semiconductor membrane", as recited in claim 1, for example.

Applicant further traverses the Office's rationale for combining Clingman et al. and Belford. The Office states: *Since Clingman et al. and Belford are both from the same field of endeavor, a method for forming a wafer, the purpose disclosed by Belford would have been recognized in the pertinent art of Clingman et al.* Applicant respectfully disagrees that Clingman et al. and Belford are in the same field of endeavor. Clingman et al. is directed toward a single crystal piezo apparatus and method of forming the apparatus (Title) using a steel layer with a preformed curvature, and is not in the field of forming a wafer used in integrated circuit fabrication on which integrated circuits are formed. Applicant respectfully asserts that the Office has not clearly articulated a rationale (accounting for different electrical and mechanical properties) for replacing the steel layer of Clingman et al. with a wafer used in integrated circuit fabrication on which integrated circuits are formed. The Office has not shown why an integrated circuit wafer would be able to flex back with sufficient force to cause a compressive prestrain to be applied to the SCP material to harden the single crystal piezo apparatus,[4] or why steel would be an appropriate integrated circuit wafer.

The Office continues: *Therefore, it would have been obvious to one or ordinary skill in the art at the time the invention was made to modify Clingman et al. by wherein the substrate wafer is a structure used in integrated circuit fabrication of which integrated circuits are formed as taught by Belford to reduce short channel effects such as source/drain parasitic resistances and velocity saturation of carriers in the channel (col. 1 lines 41-55).* Applicant respectfully traverses. The asserted rationale does not address the ability of the integrated circuit wafer to flex back to cause a compressive prestrain to be applied to the single crystal piezo material material. The rationale appears to be asserting that the strain reduces short channel effects and velocity saturation of carriers in the channel. However, Col. 1 lines 41-55 of Belford refer to MOSFETs in CMOS circuits; whereas Clingman et al. compressively strains the single crystal

---

[4] *Clingman et al.*, at col. 1 lines 14-16.

piezo material. The Office has not established that the single crystal piezo material includes MOSFETs, and is strained to reduce short channel effects and velocity saturation of carriers in the channel.

With respect to claim 1, Applicant is unable to find, in the proposed combination of Clingman et al. and Belford, a method that includes bonding the semiconductor membrane to the substrate wafer and straightening the predetermined contour to induce a predetermined strain in the semiconductor membrane, as recited in the claim. Claims 2-3, 6, 7, 12, and 14 depend on claim 1 and are asserted to be in condition for allowance at least for the reasons provided with respect to claim 1.

With respect to claim 16, Applicant is unable to find, in the proposed combination of Clingman et al. and Belford, a method that includes flexing a substrate wafer into a flexed position where the substrate wafer is a structure used in integrated circuit fabrication on which integrated circuits are formed, bonding a portion of the substrate wafer to a semiconductor layer when the substrate wafer is in the flexed position, and relaxing the substrate wafer to induce a predetermined strain in the semiconductor layer, as recited in the claim. Claims 17-20 depend on claim 16 and are asserted to be in condition for allowance at least for the reasons provided with respect to claim 16. Further, with respect to claims 19-20, Applicant respectfully asserts that "obvious to try" is an improper rationale to assert that the claimed ranges for straining the semiconductor layer applies to compressively straining the single crystal piezo material to harden the single crystal piezo apparatus.[5]

Claims 5, 21, 39-41, 44-46 and 53 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Clingman et al. (U.S. Patent No. 6,994,762) in view of Belford (U.S. Patent No. 6,455,397) and Yamazaki et al. (U.S. Patent No. 6,902,616). Applicant traverses for at least the following reasons. The proposed addition of Yamazaki et al. does not cure the deficiencies of the rejection using Clingman et al. and Belford, as identified above.

Claim 5 depends on claim 1, and is asserted to be in condition for allowance at least for the reasons provided with respect to claim 1. Claim 21 depends on claim 16, and is asserted to be in condition for allowance at least for the reasons provided with respect to claim 16.

---

[5] *Clingman et al.*, at col. 1 lines 14-16.

With respect to claim 39, Applicant is unable to find, in the proposed combination of Clingman et al., Belford, and Yamazaki et al. a method comprising forming a convex contour in a surface of a sacrificial crystalline wafer, and performing a bond cut process to form an ultra-thin semiconductor membrane and bond the ultra-thin semiconductor membrane to a substrate wafer, wherein the ultra-thin semiconductor membrane is flattened and strained when bonded to the substrate wafer, as recited in the claim. Claims 40-41 depend on claim 39, and are asserted to be in condition for allowance at least for the reasons provided with respect to claim 39.

With respect to claim 44, Applicant is unable to find, in the proposed combination of Clingman et al., Belford, and Yamazaki et al. a method comprising straining a semiconductor layer to form a strained semiconductor layer including forming a predetermined contour in one of a semiconductor layer and a substrate wafer, and bonding the semiconductor layer to the substrate wafer and straightening the predetermined contour to induce a predetermined strain in the semiconductor layer, and further comprising forming a gate separated from the strained semiconductor layer by a gate insulator, and forming first and second diffusion regions separated by a channel region where the strained semiconductor layer include the first and second diffusion region and the channel region. Claims 45-46 depend on claim 44, and are asserted to be in condition for allowance at least for the reasons provided with respect to claim 44.

With respect to claim 53, Applicant is unable to find, in the proposed combination of Clingman et al., Belford, and Yamazaki et al. a method comprising forming a strained semiconductor layer, including forming a predetermined contour in one of a semiconductor layer and a substrate wafer, and bonding the semiconductor layer to the substrate wafer and straightening the predetermined contour to induce a predetermined strain in the semiconductor layer, and further comprising forming a processor and forming a memory device in communication with the processor where forming a processor and forming a memory device includes forming at least one transistor with a channel region formed by the strained semiconductor layer, as recited in the claim.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6960 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6960

Date 11-7-07

By _____
Marvin L. Beekman
Reg. No. 38,377

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 9 day of November 2007.

LISA POSORSKE
Name

_____
Signature